Reconfigurable Electric Double Layer Doping in an MoS_2 Nanoribbon Transistor

Cristobal Alessandri, Sara Fathipour, Huamin Li, Iljo Kwak, Andrew Kummel, Maja Remškar, and Alan C. Seabaugh

***Abstract*— A back-gated multilayer nanoribbon molybdenum disulfide (MoS_2) transistor grown by chemical vapor transport and doped using polyethylene oxide cesium perchlorate is fabricated and characterized. Ions in the polymer dielectric are directed by side gates to the source and drain access regions where they form electric double layers (EDLs) that control the carrier densities. This allows the junctions of the same transistor channel to be reconfigured as an n-MOSFET, p-MOSFET, and as a tunnel field-effect transistors. The EDLs are formed at room temperature and then locked into place by cooling the polymer below the glass transition temperature (~240 K). Transport measurements are presented and explained using simulated band diagrams. Both n and p-conduction in MoS_2 is demonstrated using solid polymer ion doping, enabling characterization of a semiconductor in which the doping of the same channel has been reconfigured to form three different transistor configurations.**

***Index Terms*— Electric double layer, ion doping, molybdenum disulfide, multilayer nanoribbon molybdenum disulfide (MoS_2), tunnel field-effect transistor (FET) (TFET), TFET.**

I. Introduction

2-D SEMICONDUCTORS are being widely explored for beyond-CMOS electronics [1]. Electric double layers (EDLs) formed using solid polymers, such as polyethylene oxide (PEO) containing cesium perchlorate ($CsClO_4$), and 2-D crystals can induce degenerate sheet electron and hole densities exceeding 1×10^{14} cm^{-2} [2], [3], beyond the limits of substitutional doping in bulk semiconductors. Using PEO:$CsClO_4$, n-contact resistance as low as 200 Ω μm has been achieved in multilayer multilayer nanoribbon molybdenum disulfide (MoS_2), with a record current of 300 μA/μm at 1.6 V for a channel length of 0.8 μm [4]. As a point of reference, an n-MOSFET with a 0.5-μm gate length and biased at $V_{DS} = V_{GS} = 1.6$ V has a current of roughly 170 μA/μm [5].

While the use of electrolytes to gate transition metal dichalcogenide field-effect transistors (FETs) has been previously discussed [6]–[10] this is not the approach taken here. We use the PEO:$CsClO_4$ to dope the access regions of the transistor. Once the doping is established, the temperature is lowered to lock the ions in place. With this transistor structure, where only the access regions are exposed to the ions, the device can then be operated with a metal/Al_2O_3 back gate. This doping and locking approach using PEO:$CsClO_4$ has also been successfully applied to the formation of p-n junctions in $MoTe_2$ [11] and in WSe_2 [12]. Other approaches for n-doping [13]–[16] or p-doping [16]–[18] of MoS_2 have been reported, but here the focus is on ion doping which enables the reconfigurability.

II. Device Fabrication and Doping

The MoS_2 was grown by chemical vapor transport (CVT) from MoS_2 powder, using a two-zone furnace and an iodine transport agent [19]. This method enables the vapor-phase growth of nanotubes and nanoribbons [4], [19]. The CVT growth method is being explored to avoid the unpassivated dangling bonds that are obtained at the edges of exfoliated materials [20]. While thicknesses at the few nanometer level are desired, the nanoribbons and nanotubes produced by the CVT growth method, as currently applied, are in the range 10 ± 5 nm. The device, with cross section shown in Fig. 1, has a 13-nm body thickness and a 700-nm width. This will be referred to as a nanoribbon. The fabrication started with electron-beam (e-beam) evaporation of Ti/Au (5/100 nm) on the back of a p^+ Si wafer. The nanoribbons were tape transferred from the CVT source onto a 27-nm Al_2O_3 oxide formed by atomic layer deposition (ALD) on the wafer top surface. E-beam lithography and lift off were used to form

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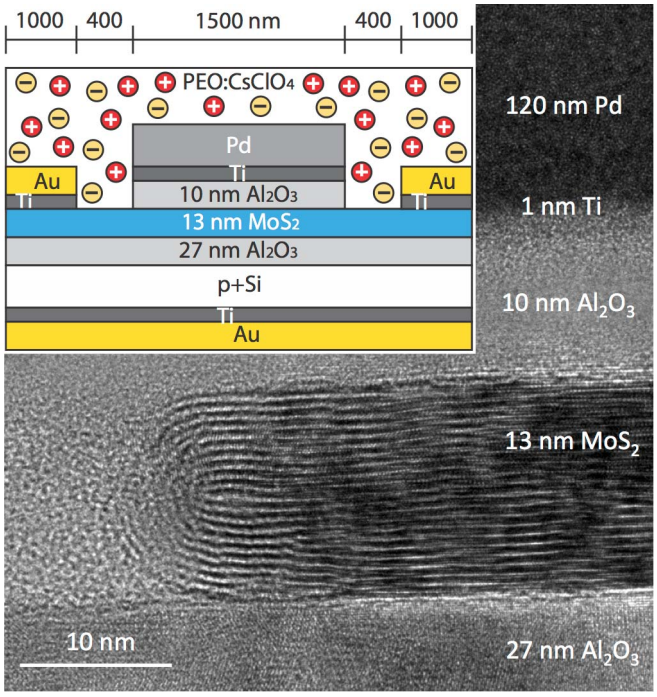

Fig. 1. Nanoribbon MoS_2 transistor cross-sectional schematic and transmission electron micrograph (TEM) along the 700-nm width. This TEM was made on completion of the measurements discussed in this paper.

Ti/Au (5/100 nm) source/drain contacts using e-beam evaporation. Side gates, not shown in Fig. 1, were also formed in the source/drain metallization step and are located 30 μm from the channel.

The ALD of Al_2O_3 on the MoS_2 nanoribbon utilized a two-step process consisting of a low-temperature physisorption step at 50 °C followed by ALD at 120 °C. In this way, conformal deposition of Al_2O_3 is achieved, wrapping around and under the nanoribbon edge without pinholes, as shown in Fig. 1. A top gate was formed by e-beam evaporation of Ti/Pd (1/120 nm), and the Al_2O_3 was etched in buffered HF using the gate as a mask to form access regions for the ion doping. The drain current was not notably reduced after etching indicating that the MoS_2 etch was insignificant. The top-gate pad away from the channel was mechanically damaged which prevented use of the gate terminal, but left the transistor fully functional when operated using the back gate.

The PEO and $CsClO_4$ were dissolved in acetonitrile and drop-cast to cover the entire surface of the wafer, followed by a 3 min anneal at 90 °C in an Ar-filled glove box. At room temperature, Cs^+ and ClO_4^- ions move on the polymer chains in the PEO in response to potentials applied between the side gates and the channel. With the source and drain grounded, a negative side gate bias V_{SG} pushes ClO_4^- ions into the channel access regions inducing hole conduction for the *p*-MOSFET. A positive side gate bias pushes Cs^+ into the access regions and induces electron conduction to set up the *n*-MOSFET. After positioning the ions with the side gates, the transistor is cooled below the glass transition temperature of the electrolyte (~240 K) to lock the ions in place and fix the doping. Measurements were carried out using an Agilent B1500 semiconductor parameter analyzer in a Cascade PLC50 vacuum probe station at 1.2×10^{-6} Torr.

Dozens of transistors have been fabricated based on this approach. The transistor reported here, however, was tested extensively over several months and represents the most thoroughly characterized of the CVT MoS_2 transistors we have tested to date. The doping results are reproducible and after locking the ions, I–V curves are reproducible with insignificant hysteresis. When the devices were reset and doped, the results were repeatable and reproducible. This device was initially tested with double sweeps and no noticeable hysteresis was observed after the ions are locked (below 220 K). The measurements reported in this paper are for single sweeps. It was verified that the polymer does not contribute any significant current below the glass transition temperature by measuring 2-μm long gaps without an MoS_2 channel and filled with PEO:$CsClO_4$. These measurements showed less than 1 pA/μm currents in the PEO:$CsClO_4$ for biases up to 4.5 V.

To provide a simple description of the connections and a consistent analysis, the left and right contacts in Fig. 1 will be referred to as the source and drain, respectively. To isolate the effect of the EDL doping on the channel, the same biasing conditions are measured for all configurations, even though for some transistor configurations this will not always be the usual transistor reporting convention.

III. MoS_2 N- and P-Doping Configurations

When polymer ion doping is used, it is essential to establish repeatable and reproducible starting conditions. Before setting the ion configuration, all the device terminals were grounded for 5 min at room temperature to reset any previous ion configuration. The EDL was then formed at room temperature by applying a potential to the side gate and grounding the drain–source, and back-gate contacts. A hold time of 0 or 3600 s (1 h) was applied before cooling at selected biases. The potentials on the terminals were maintained during cooling, which takes approximately 20 min.

Fig. 2(a) shows the transfer characteristics measured for different EDL forming conditions and for a negative drain–source bias, $V_{DS} = -0.4$ V. Following each measurement, the transistor was warmed back to 300 K, reset for 5 min and then cooled at a different side gate bias condition to set the access region doping. For $V_{SG} = 0$ V, an *n*-type FET characteristic is established, which suggests that the Fermi level is close to the MoS_2 conduction band, as is commonly observed in unintentionally doped MoS_2 [17]. Without any hold time before cooling, applying $V_{SG} = 2$ V produces a small negative shift in the threshold voltage, whereas applying $V_{SG} = -4$ V produces a slight positive shift. This is consistent with weak *n*- and *p*-type doping, respectively.

With a hold time of 1 h, a high *n*-doping is achieved with $V_{SG} = 2$ V, and back-gate modulation becomes negligible. In contrast, for $V_{SG} = -4$ V, both *n*- and *p*-branches can be observed with strong back-gate modulation. Increasing the side gate bias to −4.5 V further reduces the *n*-branch maxima, but has no significant effect on the *p*-branch maxima or the ability to back-gate the transistor.

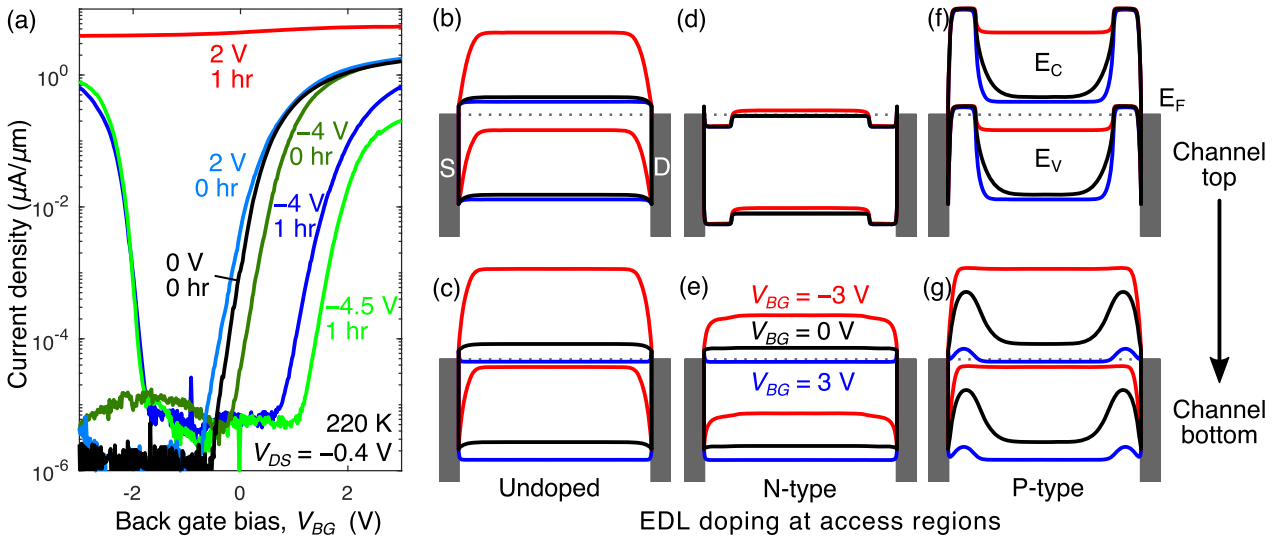

Fig. 2. (a) Measured back-gate transfer characteristics versus EDL doping condition in the transistor access regions. The EDL positions are specified by the side gate bias and hold time before cooling to freeze the ions into place. Simulated electrostatic band diagrams at the top of the channel (top row of band diagrams) and at the bottom of the channel (bottom row). The columns of band diagrams from left to right are for (b) and (c) no EDL doping, (d) and (e) n-type doping, and (f) and (g) p-type doping.

The induced carrier density from the EDL, similar to a gate, is peaked in concentration at the surface and decays with distance away from the surface. Similarly, induced carriers from the back-gate bias are maximized at the back of the MoS_2 channel and decay toward the surface. For this reason, the transport results can be expected to depend on thickness. For a thick device, independent conduction channels are induced at the surface and back-gate faces of the MoS_2. For layer thicknesses less than a Debye length in the vertical direction, the capacitances of the surface and back channels become coupled and a single conduction channel can be expected. To understand this behavior, a 2-D COMSOL multiphysics model was implemented across the channel length (source to drain) and thickness (top to bottom). The ionic charge at the access regions was modeled as a uniform fixed charge density at the PEO/MoS_2 interface of 2 and -2 μC/cm^2 for the n-doping and p-doping, respectively. These charge densities are conservative values considering measured EDL capacitances of 4 μF/cm^2 [6] have been obtained with PEO:$CsClO_4$. Electrostatic Poisson simulations were performed under different doping configurations and back-gate biases to explain the transport. Horizontal cuts of the band diagrams at the top and bottom of the MoS_2 channel are plotted in Fig. 2. Given that the channel is 13-nm thick, the effect of the ion doping is strong at the channel surface, but the back gate dominates at the bottom of the channel.

Consider the case where the ions are homogeneously distributed during cooling to arrest the ion motion, i.e., all terminal voltages are set to zero during cooling to 220 K as indicated by the black curve in Fig. 2(a). The band diagrams at the top and bottom of the channel are shown in Fig. 2(b) and (c), respectively, simulated with no surface charge in the access regions. The carrier densities are n-type both in the access regions and channel; negative back-gate bias raises the channel barrier and the measurements are consistent with the simulated band diagrams showing that the transistor turns off with over six orders of magnitude current ratio. For large, positive back-gate bias, the ON-current is likely limited by the contact barriers, and the electron concentration is peaked at the bottom of the channel.

Fig. 2(d) and (e) depicts the simulated band diagrams at the top and bottom of the channel for n-doping with $V_{SG} = 2$ V and 1 h hold time. Because of the degenerate doping induced in the access regions, the Schottky barrier is much thinner than the case shown in Fig. 2(c) and a 4× higher ON-current is observed at $V_{BG} = 3$ V. Given that the device channel is long (1.5 μm), the energy band in the middle of the channel is not determined by the doping in the access regions. Therefore, the back-gate bias should still allow modulation of the channel (far from the access regions) in the same way as in Fig. 2(b). However, the measured current shows a 20% back-gate modulation and the device cannot be turned off. The observed behavior is similar to what we observe on ion-doped and locked, back-gated transistor channels on MoS_2 [4] and WSe_2 [21] when no top gate is present. In this case the EDL controls the channel and the back-gate modulation is weak. This suggests that Cs+ ions have penetrated under the gate or in the region where the gate metal goes over the nanoribbon edge. The band diagrams computed in Fig. 2(d) and (e) follow this assumption. A recent report by Piatti *et al.* [22] using polymer ion gating indicates that Li and Na can intercalate in MoS_2 and affect channel conductance.

When a 1-h hold time is applied at room temperature for the -4 and -4.5 V side gate biases, the condition of Fig. 2(f) and (g) is achieved. A degenerate p-type doping is induced in the access regions at the top of the channel, which decays toward the bottom. Schottky tunneling of holes at the source/drain contacts should be enabled by the thin tunneling barriers. Unlike the Cs^+ doping case, the results suggest that the ClO_4^- does not intercalate or diffuse underneath the gate, which is likely because of its larger size.

TABLE I
MOBILITY AND CONTACT RESISTANCE EXTRACTED FROM BACK-GATE TRANSFER CHARACTERISTICS, COMPARED WITH RESULTS REPORTED IN THE LITERATURE. VALUES ARE REPORTED AT ROOM TEMPERATURE UNLESS OTHERWISE NOTED

	Doping type	Mobility ($cm^2/V{\cdot}s$)	Contact resistance ($k\Omega{\cdot}\mu m$)
This work	**n**	**23 at 220 K**	**<36**
Fang 2013 [13]	n	25	Not reported
Kiriya 2014 [14]	n	24.7	1
Rai 2015 [15]	n	102	0.18
Giannazzo 2017 [16]	n	11.15	Not reported
This work	**p**	**20 at 200 K**	**28**
Chuang 2014 [17]	p	Not reported	2000
Nipane 2016 [18]	p	8.4 to 137.7	Not reported
Giannazzo 2017 [16]	p	7.2	Not reported

The p-branch observed in Fig. 2(a) for negative back-gate bias is produced by lowering the hole barrier in the channel. A positive back-gate bias turns off the p-channel as expected. However, an n-branch is still observed due to conduction at the bottom of the channel, where the ion doping is weak. When increasing the side gate bias from -4 to -4.5 V during the ion configuration, the n-branch is further reduced and shifted to the right, as shown in Fig. 2(a). The p-branch has no significant change because it is mainly controlled by the channel barrier, which does not change with the doping in the access region.

Table I shows the mobility and contact resistance extracted from the transfer characteristic in linear region ($V_{DS} < V_{GS} - V_t$) using the equation $I_D = (\mu C_{OX} W/L)(V_{GS} - V_{TH})V_{DS}$, where V_{DS} and V_{GS} are corrected for the series resistance and $C_{OX} = 0.26\ \mu F/cm^2$ for 27-nm Al_2O_3 with 8.1 dielectric constant. The parameters were extracted for the p-MOSFET doped with $V_{SG} = -4$ V and 1 h hold time, and the n-MOSFET doped with $V_{SG} = 2$ V and no hold time. The n-MOSFET doped with $V_{SG} = 2$ V and 1 h hold time could not be used to extract mobility, but an upper bound for the contact resistance of 36 $k\Omega \cdot \mu m$ was estimated from the saturation current. The p-MOSFET, on the other hand, compares well with previous reports in terms of mobility and contact resistance.

IV. MoS_2 TFET CONFIGURATION

To form doping with opposite carrier types at the source and drain contacts, opposite biases are applied to the drain and source, respectively [12]. The EDL was formed at room temperature by applying $+2$ V to the drain and -2 V to the source, while the back gate was grounded. In this way, Cs^+ ions are drawn to the negative source contact and ClO_4^- ions are drawn to the positive drain contact. A hold time of 1 h was applied and the device was then cooled to 220 K while keeping the above biases. The cooling process was again approximately 20 min. After reaching 220 K, the biases were released and measurements were then taken for six temperatures between 80 and 220 K.

Under this bias condition, associated with biasing the transistor as a TFET, there is no evidence that ions of either type intercalate or diffuse under the gate. This is consistent with

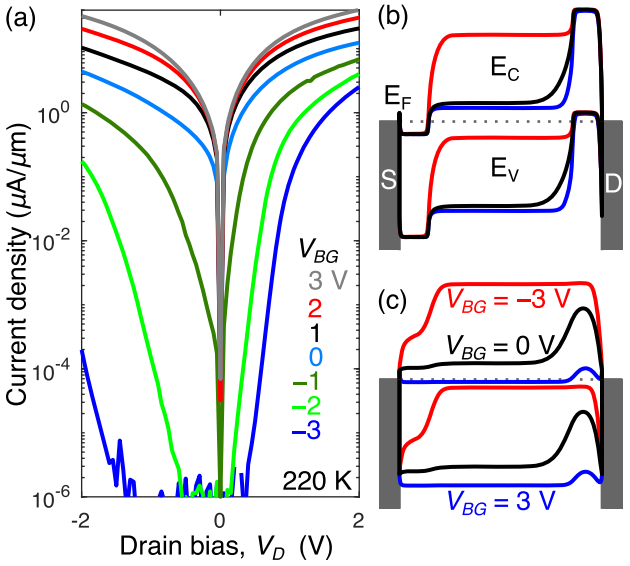

Fig. 3. (a) I_D versus V_D characteristics measured at different back-gate bias. Simulated band diagram for TFET configuration at the (b) top and (c) bottom of the channel.

simulations discussed in [12] that show that the ions accumulate adjacent to the contacts. The simulated electrostatic band diagram for the TFET configuration at the top of the channel is depicted in Fig. 3(b) as an n^+np^+ profile along the channel. The back gate modulates the channel and has no significant effect in the access regions. However, at the bottom of the channel the ion doping is weak and the back-gate modulation dominates, as shown in Fig. 3(c). Fig. 3(a) shows the $I_D - V_D$ measurements for different back-gate biases, which are readily explained by the simulated band diagrams. For large positive back-gate biases, the channel induced at the bottom dominates, so there is conduction for both negative and positive V_{DS} with almost no rectification. For zero back-gate bias, a small rectification is observed, due to the weak junction at the bottom of the channel.

The back-gate transfer characteristics measured with $V_{DS} = -0.4$ V are shown in Fig. 4(a) for different temperatures, and the subthreshold slope (SS) is shown in Fig. 4(b). At current densities below approximately $10^{-3}\mu A/\mu m$, a linear positive temperature dependence in the SS is observed, as expected in the subthreshold region, i.e., $(kT/mq)\ln(10)$, see the inset, where m is a factor related to gate efficiency. However, at current densities above $3\times10^{-3}\ \mu A/\mu m$ the swing decreases with temperature which suggests that the resistance is increasing with temperature, perhaps related to mobility degradation. No clear evidence for tunneling was observed when biased as a TFET. While high doping can be induced at the channel surface, tunneling could not be measured by back-gating the 13-nm-thick MoS_2 channel. This is because an abrupt tunnel junction could not be induced in such a thick channel.

The electrostatics of the device can be improved by reducing the channel thickness to a few monolayers to obtain a homogeneous heavy doping of the access regions and a better gate control in the channel. Although our simulations provide a qualitative understanding of the coupling between

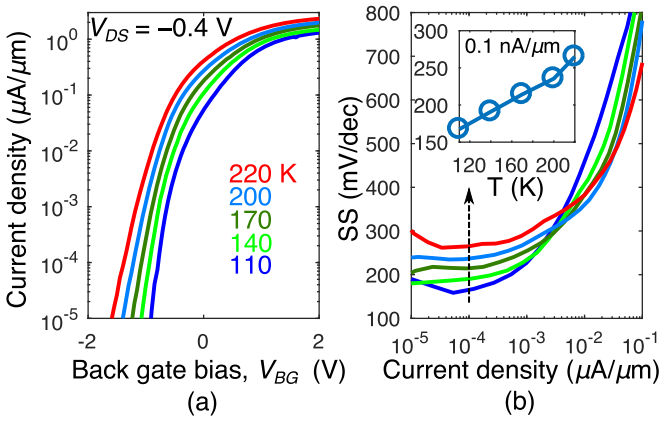

Fig. 4. (a) Temperature dependence of the back-gate transfer characteristic and (b) subthreshold swing for $V_{DS} = -0.4$ V. The inset shows the SS temperature dependence at a 10 nA/μm drain current density.

the EDL and back-gate capacitances, a more complete model is needed for a quantitative understanding, including quantum confinement effects and interlayer conduction. The use of a top gate (not operational in this device) would further improve the electrostatics for two reasons: first the top gate would modulate the doping at the top of the nanoribbon on the same plane as the EDL doping. Second, the top gate would modulate only the channel region and would not compete with the doping at the access regions as the back gate does.

V. Conclusion

Experimental measurements of EDL doping in a nanoribbon MoS_2 back-gated transistor have been presented showing *n*-MOS, *p*-MOS, and TFET configurations characterized in the same FET channel. Simulated band diagrams taking into account the front and back ends of the channel are used to explain the behavior showing that the characteristics of the 13-nm-thick channel can be readily explained. While band-to-band tunneling has been sought in these transistors for operation as TFETs, we show that the temperature dependence indicates the subthreshold transport is predominantly thermionic. To enable band-to-band tunneling, the device electrostatics must be improved by reducing the nanoribbon thickness to a few monolayers.

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